

Figure 1

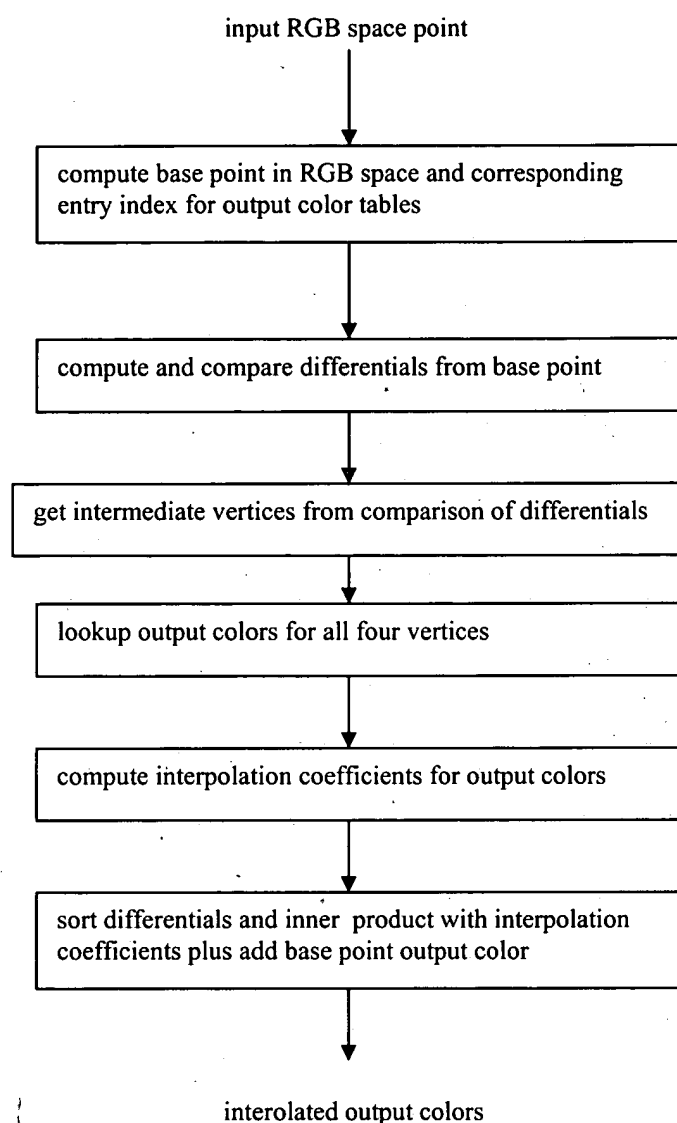


Figure 2. Pipelined datapath and multiple bank table memory architecture to achieve 1 cycle per pixel tetrahedral interpolation

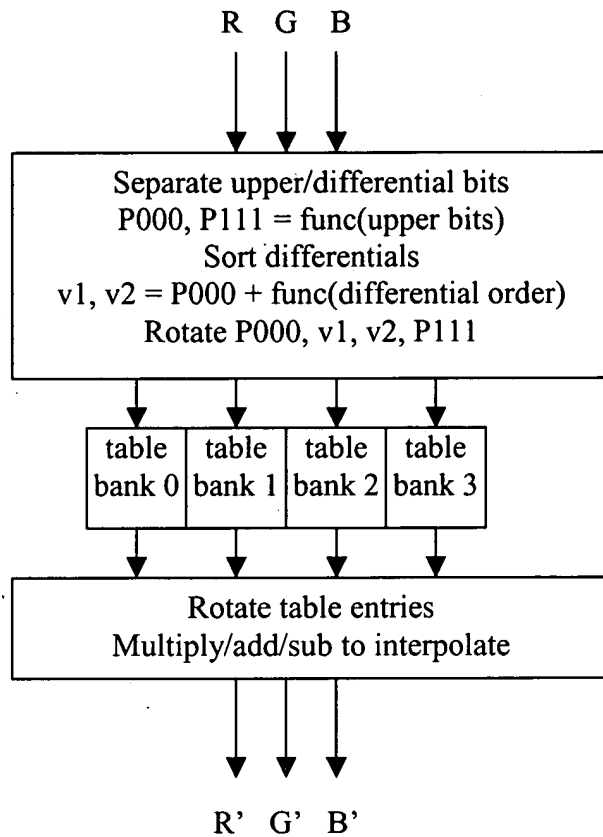


Figure 3a

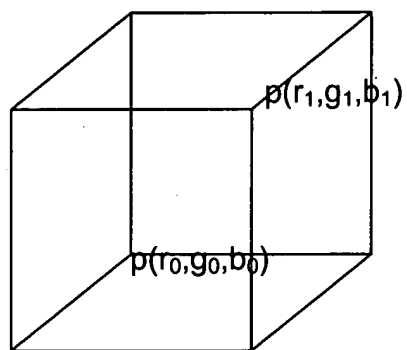


Figure 3b

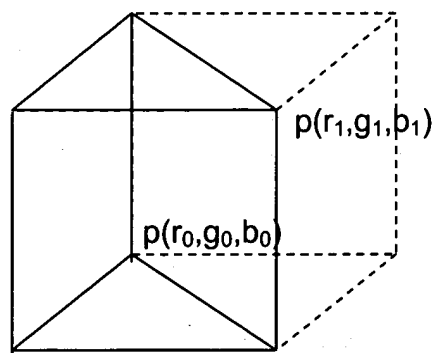


Figure 3c

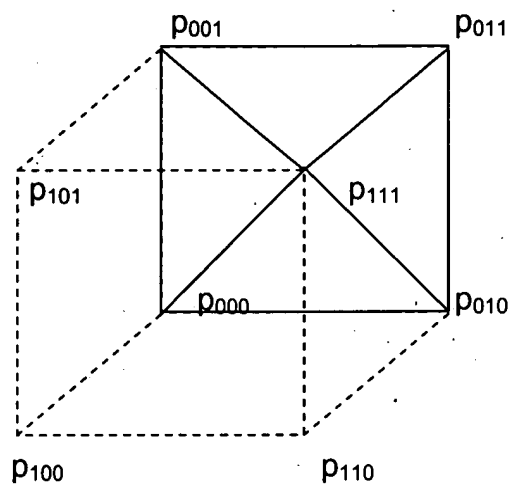


Figure 3d

